

Where Analytical Techniques Fall Short: A User's Perspective

C. Hill

Phil. Trans. R. Soc. Lond. A 1996 **354**, 2781-2793

doi: 10.1098/rsta.1996.0128

Email alerting service

Receive free email alerts when new articles cite this article - sign up in the box at the top right-hand corner of the article or click [here](#)

To subscribe to *Phil. Trans. R. Soc. Lond. A* go to:
<http://rsta.royalsocietypublishing.org/subscriptions>

Where analytical techniques fall short: a user's perspective

BY C. HILL

*GEC-Marconi Materials Technology Caswell Ltd, Towcester,
Northants NN12 8EQ, UK*

Electronic devices make enormous demands on compositional, structural and electrical characterization techniques. These demands have catalysed great technique improvements but, despite this, a large and increasing gap exists between demand and supply, especially in the characterization needs of silicon integrated circuits. These needs are outlined, the shortfall in present 1D, 2D and 3D analytical capabilities is quantitatively assessed and a strategy to bridge this gap by combining the best modelling and characterization methods is presented.

1. Introduction

Electronic materials, and the devices made from them, have made continually increasing demands on compositional, structural and electrical characterization techniques over the past 40 years. These demands have resulted in great improvements in all techniques, as described in the other papers of this volume but, despite this, in many areas a large and increasing gap exists between demand and supply. This is particularly true for the characterization needs of silicon integrated circuits, where even in bulk and 1D analysis, continual improvement in quantification, depth resolution and deconvolution of analysis artefacts is needed to keep pace with the requirements of each generation of integrated circuit technology. This is currently being achieved (see Dowsett *et al.* 1996). In multidimensional analysis, however, an immense analytical problem exists because of the complexity and non-planarity of device structures and the simultaneous sensitivity (e.g. *ca.* 1 ppm) at high spatial resolution (e.g. *ca.* $5 \times 5 \times 5 \text{ nm}^3$) often needed. Such 2D and 3D analysis of structure and composition is, however, more and more necessary to the understanding, simulation, design and control of advanced VLSI circuit components because of the increasingly 3D device structures forced on designers by device physics and materials properties when lateral dimensions are shrunk below $1 \text{ }\mu\text{m}$. The present situation is that current structures have minimum feature sizes below $0.5 \text{ }\mu\text{m}$, are very non-planar and need 2D and 3D characterization; but, at these geometries, only 1D compositional data is available of sufficient quality. The best previous compilation of 2D techniques and their capabilities is to be found in Maher *et al.* (1995); together with Pearson *et al.* (1994) and the papers in this volume, this shows that although there are several promising techniques for determining 2D carrier distributions, there is only one compositional technique that approaches the required resolution and sensitivity for determination of 2D dopant distributions (2D SIMS, Cooke *et al.* 1996). In the present paper, examples of characterization needs of some advanced VLSI structures are described,

Phil. Trans. R. Soc. Lond. A (1996) **354**, 2781–2793

Printed in Great Britain

2781

© 1996 The Royal Society

TeX Paper

the shortfall in present analytical capabilities is quantitatively assessed and a strategy to bridge this gap using a combined simulation and characterization method is presented.

The users of analytical techniques in the silicon integrated circuit industry are the engineers, technologists and scientists whose task is to design, make, optimize and manufacture semiconductor devices and circuits ultimately for commercial use. Their need for 1D, 2D and 3D compositional characterization arises because there are multidimensional aspects of the device structures and their electrical characteristics which are crucial in determining the final circuit performance, reliability and manufacturability.

Three important classes of inputs are made by analytical techniques to VLSI users: namely to process control, failure analysis and design. Inputs to process control are provided by on-line analytical tools for monitoring and controlling each step of the manufacture. These tools are necessarily non-destructive, usually based on electromagnetic radiation and must be rapid, fully automated and have sophisticated data acquisition and handling to generate the large statistical data base required for effective process control. Generally, the output is a scalar quantity (e.g. reflectivity, X-ray intensity) mapped in 2D over the whole (e.g. 200 mm) wafer. Inputs to failure analysis are provided by tools for diagnosing the physical causes of failures identified electrically in operating circuits. These are usually destructive, 2D and often involve TEM and SEM, which allow the analysis to be located to submicron accuracy in the device structure. These two inputs, though important (Fabry *et al.* 1993), lie outside the scope of this paper and will not be further considered. The class of input with which we are concerned is that of input to design, which provides the basic data from which reliable and accurate physical models, simulators and optimizers of the device and its fabrication process can be developed and maintained.

2. Analytical input to design

A modern integrated circuit is a 2D assemblage of a very large number of identical building blocks, themselves 3D on a micron scale. The building blocks are interconnected electrically by a 3D overlay of up to five metal wiring layers. It is the individual building blocks for which analysis is most crucial, but also most difficult, since they require the highest analyte sensitivity combined with the highest spatial resolution. Ideally, the engineer would have a full 3D characterization of structure and dopant distribution within the device building block, from which, using a 3D device simulator, he could predict and optimize the device electrical performance. In practice, he usually simulates the device structure in 2D with a process simulator, but he has few ways of validating this by analysing the fabricated structure adequately in 2D, and none in 3D. What is deemed 'adequate characterization will differ for each device and application, but some idea of the analysis capability required can be gathered from two representative examples from advanced device technology shown in figures 1 and 2.

The analytical sensitivity and resolution required are ultimately determined by the specified tolerances of device electrical parameters. The relationships between these for a MOS device with graded compositional profiles in the source/drain regions and channel length of about 0.35 μm , as used in the currently most advanced production CMOS processes, are shown in figure 1 and table 1, based on the analysis of Duane *et al.* (1995). For instance, specification of control of the voltage at which the device

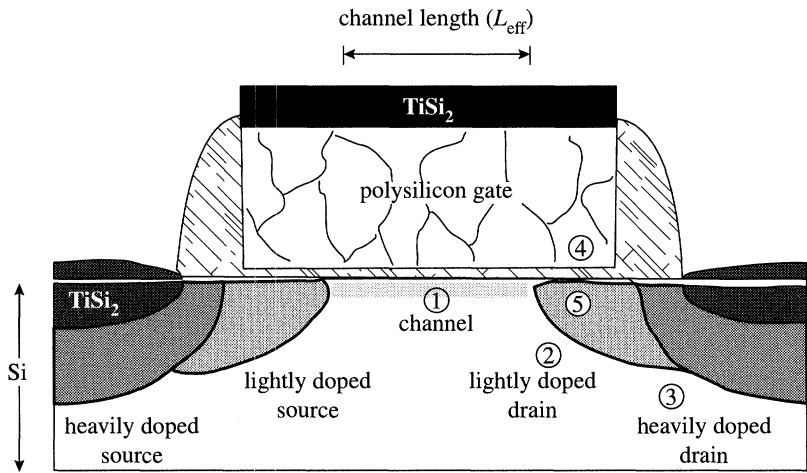


Figure 1. Schematic 2D section through a sub 0.5 μm MOS transistor, showing some areas of critical device parameter tolerance, which in turn require control of process and analytical parameters to the close tolerances shown. Data are shown in table 1.

Table 1. Typical data for the MOS transistor shown in figure 1 (Duane et al. 1995)

device tolerance	process and analysis tolerance
ΔV_t 50 mV	channel doping 1D $1\text{E}17$ and 6 nm
ΔV_t 50 mV	LDD doping 2D $4\text{E}17$ and 7 nm
Δ standby power 20%	drain junction depth 1D $2\text{E}16$ 3 nm
Δ circuit speed 20%	position of LDD relative to gate 2D $1\text{E}17$ 20 nm
lifetime > 10 years	exponential dependence of hot carrier failure on 1D peak position

turns on (ΔV_t) to 50 millivolts, implies a control of channel doping and spatial location (and hence analytical sensitivity and resolution) of 1×10^{17} atoms cc^{-1} and 6 nm in depth. The same electrical specification also implies the capability to characterize the 2D distribution of dopant in the lightly doped drain (LDD) region, to 4×10^{17} atom cc^{-1} and $7 \times 7 \text{ nm}^2$ spatial location. An example from a more advanced CMOS device in the research stage is shown in figure 2, based on the work of Hori et al. (1994). The very short channel length of $0.05 \mu\text{m}$ gives the the device, when used as a building block, the potential for a circuit with very high switching speed and packing density. To realize this potential, very careful engineering of the 2D dopant distributions in the source and drain regions of the device is mandatory, since the electric fields must be graded (to avoid avalanche multiplication), and simultaneously the junction capacitances must be minimized (for speed) and the depletion layers at the drain edges kept as narrow as possible (to maintain the specified turn-on voltage). The devices in figure 2 achieve this by incorporating two different types of

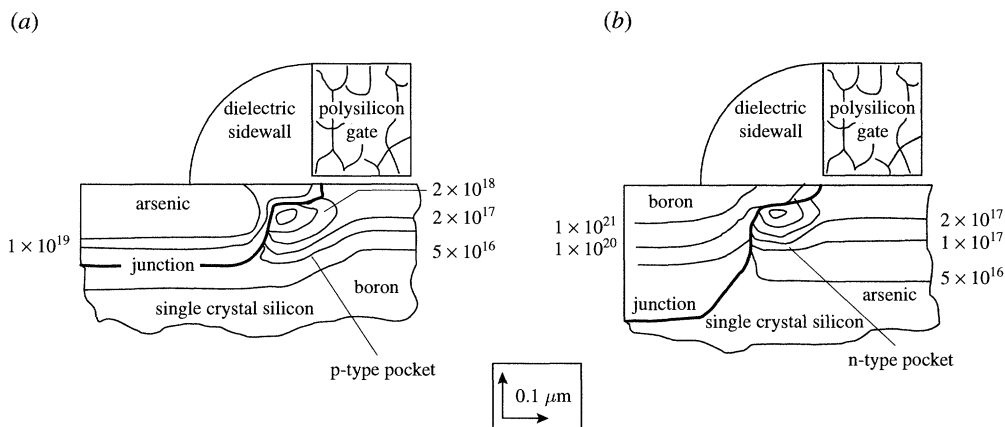


Figure 2. Schematic 2D section through the drain regions of advanced CMOS transistors with sophisticated source-drain engineering. The placement of, and exact 2D dopant distributions within, the implanted 'pocket' regions, are crucial to device operation; to characterize these requires 2D analytical capability of $1 \times 10^{17} \text{ cc}^{-1}$ and $5 \times 5 \text{ nm}^2$: (a) NMOS transistor drain region; (b) PMOS transistor drain region. Adapted from Hori *et al.* (1994).

small, but exactly specified, 2D doped zones. Lightly doped shallow 2D extensions to the heavily doped source drain, using implantation of As^+ (NMOS) and BF_2^+ (PMOS), followed by anneal, help to grade the electric field and, in addition, deeper 2D 'pockets' of opposite doping type (As^+ in PMOS and BF_2^+ in NMOS), created by implantation and anneal, define narrow and small area lateral depletion layers. The device performance is sensitive to the exact placement of these zones in the device and to the dopant distribution within these zones, so that characterization of these structures requires at a minimum simultaneous 2D determination of sensitivity $1 \times 10^{17} \text{ cc}$ and resolution $5 \text{ nm} \times 5 \text{ nm}^2$.

So far we have only considered the doping distributions and structure in the 2D sections through CMOS devices in the plane of current flow. For many devices, characterization of this section is sufficient to determine the major electrical characteristics. Increasingly, however, the optimization of smaller devices is forcing a reduction in device lateral dimensions without a proportional scaling vertically, and this often means that the 3D corners of device structures are significantly affecting performance, through, for example, increased electric field or capacitance.

3. The shortfall in analytical capability

The task of characterising regions of devices increases rapidly in difficulty as the dimensionality changes from 1 to 2 to 3D, since the number of atoms available for analysis at each data point decreases and the minimum number of data points for adequate description of the region increases, as the power of dimensionality gets larger. These strict criteria can be relaxed somewhat for many devices by using symmetry and taking into account the lower sensitivity of the device to 2D and 3D dopant distributions than to 1D profiles.

A typical assessment for an MOS transistor gate region is shown in figure 3, which gives the smallest domain sizes for adequate characterization of the 1-, 2- and 3D regions of the structure in terms of the minimum feature size L . These domain sizes, when combined with typical resolution data determined from device studies

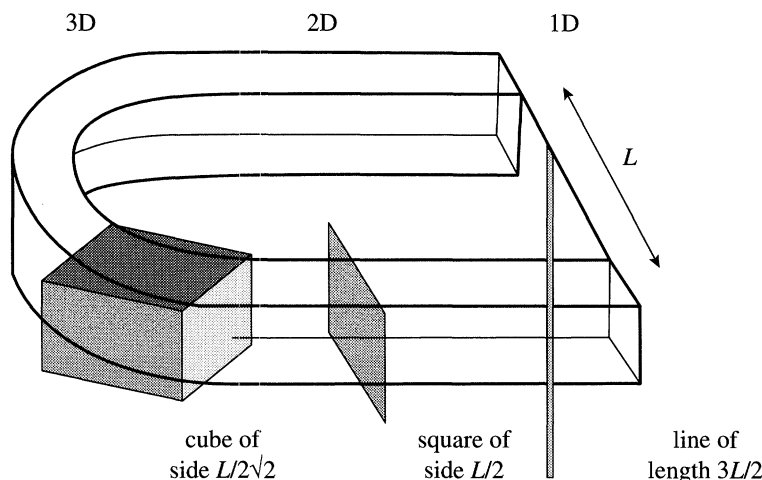


Figure 3. Schematic diagram of a minimum feature size (L) region of a CMOS VLSI transistor. One such region is the part of the source adjacent to the gate, which region is doped throughout, with a distribution that varies vertically (1D) in the central area, vertically and laterally (2D) at the edges, and in 3D at the corners. The diagram shows the minimum dimensions of analysis domains for adequate characterization of these three areas of the structure. With $L = 0.3 \mu\text{m}$, and the spatial resolutions given in table 2 for 1D, 2D and 3D analysis, this implies a minimum number of data points of about 200, 800 and 1250 for the 1D, 2D and 3D domains, respectively.

of the kind illustrated in figures 1 and 2, give a minimum number of data points for 1, 2 and 3D characterization. Taken together with sensitivity figures from the same source, this data allows the ideal characterization technique to meet VLSI needs to be defined, with a simultaneously obtainable combination of sensitivity (S), resolution (Re) and speed of data acquisition (Ra) specified, and a figure of merit $Ra/(S \times Re)$ quantified. Table 2 summarizes these ideal parameters for 1D, 2D and 3D compositional analysis of minority components and compares them with the same parameters for some actual analytical techniques.

It is clear from table 2 that only in 1D profiling does an actual analysis technique approach the characteristics of the ideal. 1D SIMS falls short mainly on speed of data acquisition, and this is an acceptable penalty where high depth resolution is essential. In 2D dopant distribution measurement, even the best techniques, STM and 2D SIMS, have a figures of merit less than 1% of the ideal value; STM gives only a semi-quantifiable carrier density which cannot be uniquely related to compositional concentration; 2D SIMS does not, so far, quite reach the necessary spatial resolution and can only be carried out on special structures (Cooke *et al.* 1996). In 3D dopant distribution measurement, the situation is far worse; scanning Auger electron spectroscopy has the best figure of merit, meeting the resolution requirements but failing the sensitivity requirement by a factor of 1000 and the speed requirement by at least a factor of 20. Thus, for majority components, scanning AES, and the sophisticated 3D technique based on it (MULSAM, Prutton *et al.* 1991), are slow compared with the ideal, but otherwise satisfactory; for minority components, there is no satisfactory technique available and no present developments known likely to provide one in the future, as shown by the papers in this volume. Since table 2 shows that there are only 0.1 analyte atoms in the ideal resolved volume ($10 \times 10 \times 10 \text{ nm}^3$) at the ideal sensitivity (10^{17}), this is perhaps not surprising.

Table 2. *Comparison of some parameters of the more promising techniques for 1D, 2D and 3D compositional analysis, compared with those of the ideal technique required by silicon VLSI technology*

Figures of merit are only approximate, since exact values depend on the particular element, matrix, equipment characteristics and mode of use, and may vary by an order of magnitude from those shown here. This does not affect the main conclusion, that the gap between the characteristics of ideal and actually available 3D techniques is many orders of magnitude. Dimension x is always normal to the sample surface, directions y and z are mutually orthogonal directions parallel to the surface plane. Data for comparable charge carrier mapping techniques is shown in *italics*. (Data based on this volume and recent literature.)

technique	can be applied to		analysis parameter combinations that are simultaneously achievable			approx. figures of merit		
	structures	elements	sensitivity (atoms/cc) S	resolution Re	speed Ra	number of analyte atoms	analysis time min	figure of merit $Ra/(S \times Re)$
elemental analysis								
3D				$\text{nm} \times \text{nm} \times \text{nm}$	voxels min^{-1}		for 1250 voxel	voxels $\text{atom}^{-1} \text{min}^{-1}$
ideal method	actual device	all	1E17	$10 \times 10 \times 10$	20	0.1	62	200
imaging SIMS	actual device	all	1E17	$500 \times 500 \times 10$	< 1	250	> 1250	< 0.004
scanning AES	actual device	all (-H)	1E20	$10 \times 10 \times 5$	< 1	50	> 1250	< 0.02
EDX on XTEM	actual device	all (-H)	5 E20	$5 \times 5 \times 5$	1	60	1250	< 0.015

Table 2. *Cont.*

technique	can be applied to		analysis parameter combinations that are simultaneously achievable			approx. figures of merit		
	structures	elements	sensitivity (atoms/cc) S	resolution Re	speed Ra	number of analyte atoms	analysis time min	figure of merit $Ra/(S \times Re)$
				nm \times nm ($z = \text{nm}$)	pixels min ⁻¹		for 800 pixel	pixel cm atom ⁻¹ min ⁻¹ $\times 1E6$
2D								
ideal method	actual device	all elements	1E17	5 \times 5 ($z = 1000$)	20	2.5	40	800
imaging SIMS	actual device	all	1E17	200 \times 200 ($z = 500$)	< 1	2000	> 800	< 0.025
scanning AES	actual device	all (–H)	1E20	10 \times 10 ($z = 5$)	< 1	50	> 800	< 1
EDX on XTEM	actual device	all (–H)	5 E20	5 \times 5 ($z = 50$)	< 10	625	> 80	< 0.016
2D SIMS	special structure	all	1E16	30 \times 30 ($z = 300 \times 30$)	1	80	800	11
STM	actual device	all	5E22	0.2 \times 0.2 ($z = 2$)	< 10	1	> 80	<i>i0.5</i>
nano SRP	actual device	charge carriers	1E16	50 \times 50 ($z = ?$)	< 1	—	> 800	<i>i4</i>
selective etch + ATM	actual device	charge carriers	3E17	25 \times 25 ($z = 40$)	< 1	—	> 800	<i>i0.5</i>

Table 2. *Cont.*

technique		can be applied to		analysis parameter combinations that are simultaneously achievable			approx. figures of merit		
elemental analysis	structures	elements	sensitivity (atoms/cc)	resolution <i>R_e</i>	speed <i>R_a</i>	number of analyte atoms	analysis time min	figure of merit <i>R_a/(S × R_e)</i>	
1D				nm (<i>y, z</i> = nm)	layers min ⁻¹		for 200 pixel	layer cm ² atom ⁻¹ min ⁻¹ × 1E12	
ideal method	actual device	all elements	1E16	2 (<i>y, z</i> = 1000)	5	20	40	2500	
1D SIMS	actual device	all elements	1E16	5 (<i>y, z</i> = 1000)	1	50	200	200	
profiling AES	actual device	all (–H)	5E19	1 (<i>y, z</i> = 1000)	5	5000	40	10	
<i>SRP</i>	<i>actual device</i>	<i>charge carriers</i>	<i>1E16</i>	<i>5</i>	<i>10</i>	—	<i>20</i>	<i>2000</i>	
ideal method	special structure	all elements	1E14	1 (<i>y, z</i> = 1E6)	10	10 000	20	1 000 000	
RBS	special structure	all > matrix mass	5E19	10 (<i>y, z</i> = 1E6)	5	5E9	40	0.1	
1D SIMS	special structure	all elements	1E14	2 (<i>y, z</i> = 1E5)	10	500	20	50 000	

4. A characterization strategy

Since, despite the wealth of excellent 2D and 3D characterization techniques available, the foregoing analysis has shown that these are not directly applicable to the analysis of minority elements in silicon in actual VLSI structures, is there any way to get the input to device design so badly needed? A possible method is proposed here.

This approach involves the use of technology simulation, calibrated with good characterization data, which may come from any of the techniques in table 2. 2D technology simulation has reached a high level of sophistication (Ryssel & Pichler 1995), and at high spatial resolution the capability to generate a simulated structure which shows the complete 2D doping element distributions is much closer to the ideal than is the capability to directly measure such a structure. This can be seen from the data in table 3, based on experience with technology simulators such as SUPREM4, STORM, IMPACT; in 1D and 2D, the figures of merit of the actual simulation techniques are better than, or equivalent to, the ideal values. There is, as yet, no generally available 3D technology simulator, but the several approaches in development (Lorenz 1995) and the increasing demands of technology are likely to provide one in the future. Such a simulator could meet the needs of sensitivity and resolution and, using present workstation capability, would only fail to meet the figure of merit because of speed; the continuing improvements in computing performance will close this gap in time.

If a simulator is to be used in this way, to provide reliable data to designers about any VLSI structure that the technology can in principle fabricate, then it must be based on models which embody the correct physics and chemistry of the processes, and it must be accurately calibrated over the whole experimental field to which it will be applied. Currently available simulators need considerable improvement in at least one of these areas. All characterization techniques can contribute to this, since the physics and chemistry can often be established at a larger scale and lower sensitivity than that of the device structure and the calibration can be effected by a carefully targeted combination of many 1D, several 2D and a few 3D measurements. The use of special structures to obtain the best data is quite acceptable, since a few such structures will yield data that will be used (through the simulator) to predict very many actual device structures at a much smaller scale. The procedure is to use the simulator to simulate the calibration structures, to predict the analytical measurement data, to compare this to the actual data and to optimize the parameters of the simulator until the two sets agree.

Although all analytical techniques can make valuable and complementary inputs to this approach, to do so they must satisfy a number of essential criteria. Firstly, a vital component of this method is to include simulation of the experimental response function in predicting the experimental data, so that one is comparing like with like. Much simulator calibration in the past has omitted this crucial step, comparing, for example, simulator output with raw SIMS data. A proper procedure for boron diffusion model calibration by SIMS is described in Jones *et al.* (1993), in which, by convoluting the SIMS measurement response function with the delta-doping profile of an experimental Si-Ge layer, the experimentally measured broadened profiles are shown to result from entirely different causes. In the case of boron, there is real and quantifiable solid state diffusion, whereas in the case of the germanium, there is no measurable diffusion and broadening is solely due to the SIMS response function. Secondly, in recording and publishing analytical data, full details of both the

Table 3. Comparison of the characteristics of the ideal techniques for determining dopant distribution in 1D, 2D or 3D, with those achievable by simulation

The figures of merit show that simulation meets the ideal requirements for 1D and 2D dopant distributions, and approaches the ideal for 3D much closer than measurement techniques. A key factor not included in this table is the accuracy of the simulation; this depends crucially on the relevance and calibration of the simulator for the particular technological situation and number of dimensions, and requires characterization. This characterization can use special structures, and does not have to simultaneously achieve highest resolution and sensitivity; thus techniques can be used for which the figures of merit are far from the ideal value.

technique of determining the dopant distribution	structure capable of being determined	elements that can be determined	sensitivity S	resolution Re	speed Ra	number N	time for analysis (min)	figure of merit $Ra/(S \times Re)$
3D			atoms cc^{-1}	$nm \times nm \times nm$	voxels min^{-1}	of analyte atoms	for 1250 voxels	voxel $atom^{-1} min^{-1}$
ideal	actual device	all elements	1E17	$10 \times 10 \times 10$	20	0.1	62	200
simulation	actual device	all doping elements	1E16	$5 \times 5 \times 5$	0.001	0.01	1.25E5	8
2D			atoms cc^{-1}	$nm \times nm$ ($z = nm$)	pixels min^{-1}	of analyte atoms	for 1250 pixels	pixel $cm atom^{-1} min^{-1} \times 1E6$
ideal	actual device	all elements	1E17	5×5	20 ($z = 1000$)	2.5	40	800
simulation	actual device	all doping elements	4E16	5×5	6 ($z = 1000$)	0.25	200	600
1D			atoms cc^{-1}	nm ($y, z = nm$)	layers min^{-1}	of analyte atoms	for 200 layers	layer $cm^2 atom^{-1} min^{-1} \times 1E12$
ideal	actual device	all elements	1E16	2	5 ($y, z = 1E6$)	20	40	2500
simulation	actual device	all doping elements	1E15	1	5	1	40	50 000

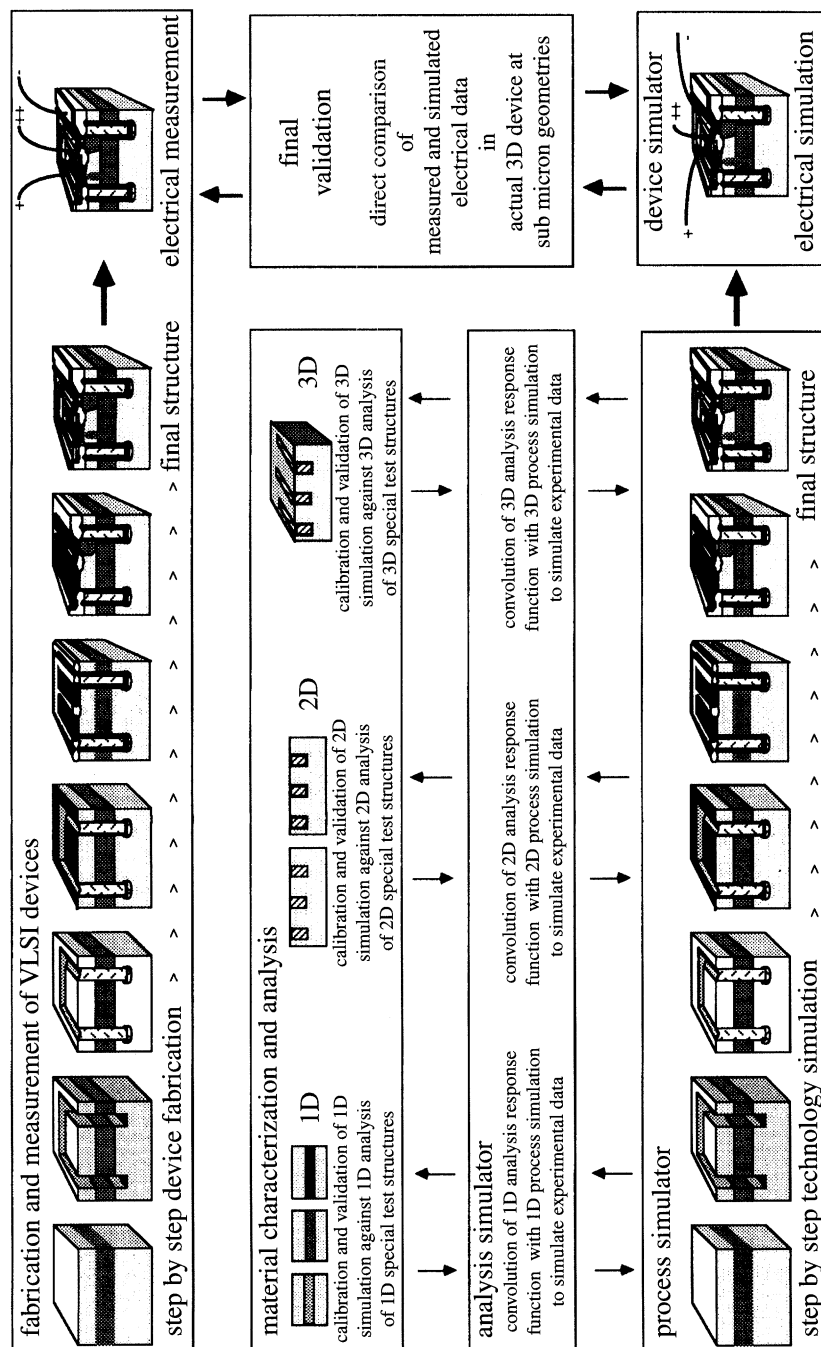


Figure 4. Schematic representation of the combined use of analysis and simulation tools to determine 1D, 2D and 3D dopant distributions in submicron VLSI device structures. The device building block represented is $5 \times 5 \times 5 \mu\text{m}^3$ volume containing the core (transistor + isolation trench) of a $0.5 \mu\text{m}$ bipolar technology. The use of analysis tools on special structures at larger geometries to develop and calibrate correct physical models, and the final comparison of measured and simulated electrical data on the actual device structures, gives confidence in the process simulator for prediction of 3D dopant distributions at submicron geometries.

process technology by which a structure was fabricated, and of all the analytical conditions, including the instrumental response function, must be given. If either of these is missing, the data is insufficiently well-characterized to be used for simulator calibration. Thirdly, this procedure implies and requires a close collaboration and communication between experts and developers of the analytical techniques and of

the technology simulators; neither can now work usefully in isolation. A summary of the whole combined characterization and modelling strategy is given schematically in figure 4, using, as an example, application to a generic 0.5 μm geometry bipolar VLSI technology.

The prognosis for the success of this approach is good. VLSI engineers are already used to using simulation tools routinely for visualizing, designing and optimising device structures in 1D and 2D, and will use 3D tools as soon as they are commercially available. There is thus already a strong driving force for accurate, reliable and well-calibrated process simulators. The normal approach also gives a powerful method of checking the combined accuracy and correctness of the characterization techniques and process models used to generate the simulated structure, by using that structure in device simulators (which are simpler and better calibrated than process simulators) to predict the electrical characteristics of the device. These characteristics can be measured to very high accuracy (1 ppb) over a very wide range (10^9), and compared to the simulation to provide final validation of the whole simulation and characterization process, shown schematically as the last step in figure 4. Where the comparison is poor, this shows the need for a better simulation chain. Detailed comparison of process simulation and compositional characterization data at each step can then identify, quantitatively and specifically, where improvement is required; which may be in the simulators (e.g. physical models, model calibration, simulator construction) or analyses (e.g. sample design, analysis technique). This provides a methodology by which the areas for continuous improvement in analysis techniques and in simulators, necessary for development of VLSI technology, can be identified and specified.

5. Conclusions

Silicon VLSI technology needs accurate inputs to design from 1D, 2D and 3D compositional characterization and from simulation. There is a serious present and future shortfall in 2D and 3D analytical techniques for this purpose. The excellent progress made in analytical techniques as described in the other papers in this volume has not been sufficient on its own to close this gap, as can be seen by comparing their sensitivity, resolution and speed with the analytical requirements quantified in this paper. A strategy to overcome this problem is proposed, in which a close combination of characterization techniques and simulation techniques is used to predict reliable and accurate 2D and 3D dopant distributions. Continuous improvement in both compositional analysis and in simulator relevance and accuracy can be expected from this approach.

This paper is based on work published by myself and colleagues in the Silicon Modelling Group at Caswell over the past five years and supported financially by GEC Plessey Semiconductors, GEC Marconi Materials Technology Ltd and the European ADEQUAT project; all of these are thanked for permission to publish.

References

- Cooke, G. A., Pearson, P., Gibbons, R., Dowsett, M. G. & Hill, C. 1996 Two-dimensional profiling of large tilt angle, low energy boron implanted structure using secondary ion mass spectrometry. *J. Vac. Sci. Technol. B* **14**, 348–352.
- Duane, M., Nunan, P., ter Beek, M. & Subramanyan, R. 1996 Dopant profile control and metrology requirements for sub 0.5 micron MOSFETS. *J. Vac. Sci. Technol. B* **14**, 218–223.

- Fabry, L., Köster, L., Pahlke, S., Kotz, L. & Hage, J. 1993 Contamination monitoring and analysis methods in large-scale silicon manufacturing. In *Proc. of Crystalline Defects and Contamination: Their Impact and Control in Device Manufacturing*, pp. 193–221. Pennington, NJ: The Electrochemical Society.
- Hori, A., Nakaoka, H., Umimoto, H., Yamashita, K., Takase, M., Shimizu, N., Mizuno, B. & Odanaka, S. 1994 A 0.05 μm -CMOS with ultra-shallow source-drain junctions fabricated by 5 Kev ion implantation and rapid thermal annealing. In *Proceedings of IEDM*, pp. 19.1.1–19.1.4. Piscataway, NJ: IEEE.
- Jones, S. K., Hill, C., Nigrin, S., Manson, A. J. & Dowsett, M. G. 1994 A new calibration method for dopant diffusion models applied to silicon heterobipolar technology. In *Proc. ESSDERC 1994* (ed. C. Hill & P. Ashburn), pp. 85–87. Paris: Edition Frontieres.
- Lorenz, J. H. (ed.) 1995 *Three-dimensional process simulation*. Vienna: Springer.
- Mathur, R., Ehrstein, J., McGuire, G. (eds) 1996 Third international workshop on the measurement and characterisation of ultra-shallow doping profiles in semiconductors. *J. Vac. Sci. Technol. B* **14**, 190–462.
- Pearson, P. J., Hill, C., Allen, R. W. & Robbins, D. J. 1994 Automated lateral junction measurement in integrated circuit structures to 30 nm precision. In *Proc. ESSDERC 1994* (ed. C. Hill & P. Ashburn), pp. 597–600. Paris: Edition Frontieres.
- Prutton, M., Walker, C. G. H., Greenwood, J. C., Kenney, P. G., Dee, J. C., Barkshire, I. R., Roberts, R. H. & El Gomati, M. M. 1991 A third generation Auger microscope using parallel multispectral data acquisition and analysis. *Surf. Interf. Analysis* **17**, 71–84.
- Ryssel, H. & Pichler, P. (eds) 1995 *Simulation of semiconductor devices and processes*, vol. 6. Vienna: Springer.